VC SpyGlass Lint

Early design analysis for logic designers

Overview

Inefficiencies during RTL design development usually surface as critical design bugs during the late stages of design implementation. If detected late, these bugs often lead to a large number of iterations; if left undetected, they can lead to expensive silicon respins. The VC SpyGlass™ RTL Signoff platform, builds on the proven SpyGlass® technology for early design analysis with the most in-depth analysis at the RTL design phase. VC SpyGlass provides an integrated solution for analysis, debug, and fixing with a comprehensive set of capabilities for structural and electrical issues, all tied to the RTL description of the design.

Introduction

With increasing complexity and the size of chips, achieving predictable design closure is a challenge. A multitude of coding styles, structural and electrical design issues can manifest themselves as design bugs, resulting in design iterations, or worse—silicon respins. Other tools may detect design bugs but often at late stages of design implementation, after a significant investment in time and effort has already been made. As design teams become geographically dispersed, consistency and correctness of design intent become a key challenge for chip integration teams. Emphasis on design reuse and IP integration requires that design elements be integrated and meet guidelines for correctness and consistency within a shorter span than necessary.

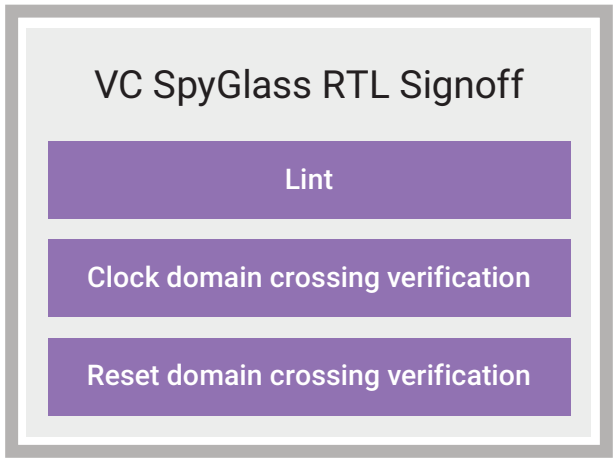

Figure 1: VC SpyGlass RTL Signoff solution

VC SpyGlass Lint: Structural RTL Checks

The VC SpyGlass linting solution integrates industry-standard best practices with Synopsys' own extensive experience working with industry-leaders. Lint checks include design reuse compliance checks such as STARC and OpenMORE to enforce a consistent style throughout the design, ease the integration of multi-team and multi-vendor IP, and promote design reuse.

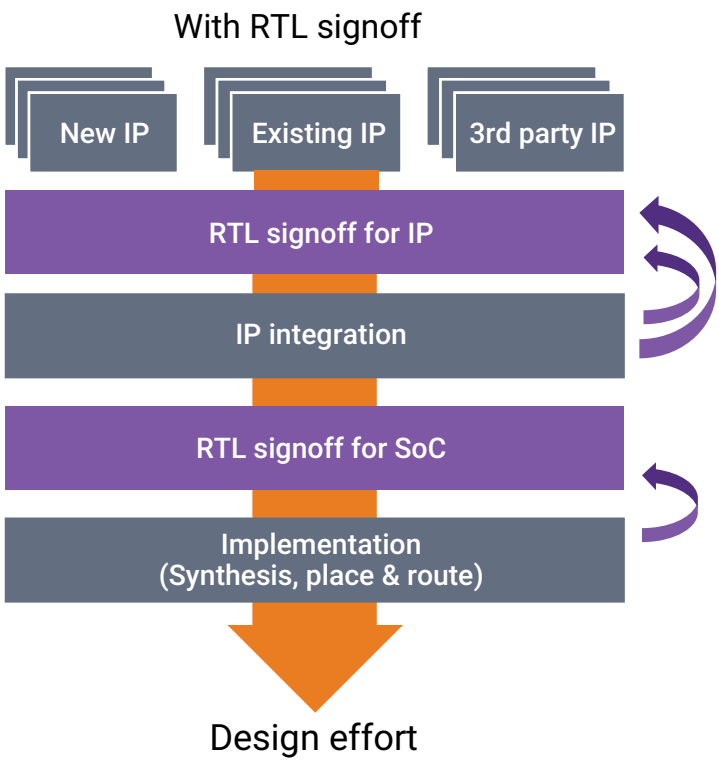

Figure 2: VC SpyGlass delivers reduced iterations, design effort and schedule risk

Smarter, Faster and Deeper Analysis

VC Synopsys Lint provides a three-pronged attack on the issues preventing RTL signoff:

1. Higher debug productivity through low noise structural analysis using an efficient and robust synthesis engine along with smarter analysis with compressed messaging
2. Extensive coverage of language and structural checks used to identify and fix issues earlier in the flow
3. Deeper analysis using formal technology to mitigate functional errors on corresponding structural lint rules and removal of uncertainty by providing conclusive results

Noise Reduction and Improved Accuracy of Results Using Formal Techniques

VC SpyGlass Lint uses advanced formal techniques to pinpoint deeper functional problems in RTL designs without requiring test benches or assertions. The integrated solution of traditional linting technology with formal technology leverages the comprehensive and widely used lint checks within the formal flow resulting in noise reduction and improved accuracy of results.

The formal aware lint coupled with the increased ease of use results in advanced debugging and interactivity.

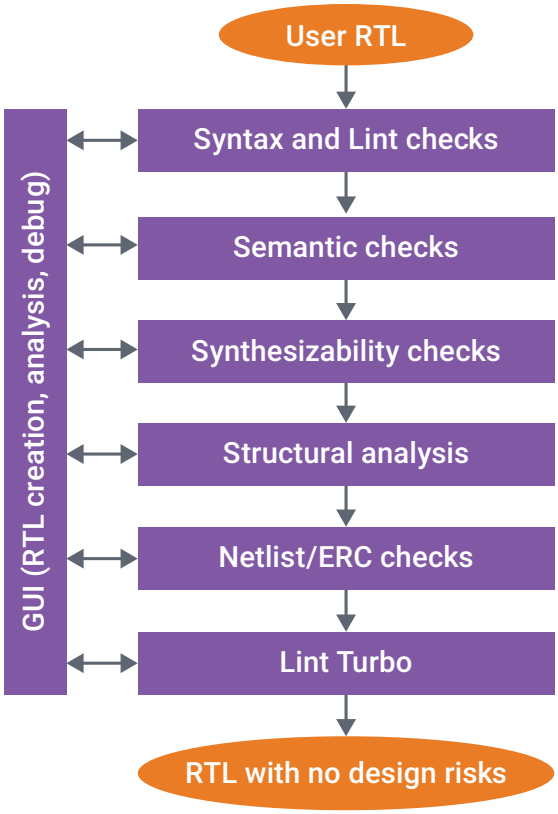

Figure 3: VC SpyGlass Lint checks for RTL analysis

Early Detection of Implementation Challenges

The VC SpyGlass Lint solution dramatically reduces the inherent risk in developing first-pass complex multimillion-gate, nanometer-scale SoCs by accurately detecting design issues at the RTL level. It flags almost all areas of the design that are likely to present implementation challenges.

- Identify critical design issues in RTL with sophisticated static and dynamic analysis
- Integrated comprehensive set of electrical rules check to ensure netlist integrity
- Enables design reuse compliance checks, such as STARC and OpenMORE to enforce a consistent style
- Step-by-step framework to capture and automate customer specific design rules
- Native integration with Verdi® provides a debug environment to enable easy cross-probing between violation reports, schematic and RTL source
- Supports Verilog, VHDL, SystemVerilog and mixed-language designs
- Tcl shell for efficient rule execution and design querying
- SoC abstraction flow for faster performance and low noise

Advanced Methodology

VC SpyGlass Lint provides a structured, easy-to-use, and comprehensive method for solving RTL design issues, thereby ensuring high-quality RTL with fewer but meaningful violations.

- GuideWare™ methodology documentation and rule-sets included
- Infrastructure for rule selection and customization aligned with design milestones
- Guided steps for completing a series of recommended steps to ensure design compliance to HDL standards, coding style, synthesis, simulation, verification, connectivity, clock and reset issues
- Step-by-step approach detects and fixes design bugs in alignment with design milestones, and ensures predictable design closure without any last-minute surprises or a high volume of violations

Seamless Integration Increases Efficiency

VC SpyGlass Lint supports “correct-by-construction” design, leading to early design closure and minimizing costly back-end debugging and iterations.

- Directly integrated advanced VC SpyGlass CDC and VC SpyGlass RDC capabilities
  - Fast path to productivity for non-experts
  - Structured methodology enables quick adoption by engineers and constraints-optimized designs
- Reduces or eliminates the need for respins
- Enables early closure of hand-off ready RTL design reducing iterations later in flow
- Elevates design optimization from gate-level to RTL
- Helps dispersed design teams to create more consistent, high-quality designs
- Enables effective design reuse and IP integration
- Integrates seamlessly into existing design environments enhancing efficiency

VC SpyGlass Lint integrates industry-standard best practices with Synopsys’ own extensive experience of working with industry-leaders.

For more information about VC SpyGlass Lint and the rest of the VC SpyGlass RTL Signoff platform, visit www.synopsys.com or contact your local sales representative.